CIIC 3081 - Course Syllabus

1. General Information:

Alpha-numeric codification: CIIC 3081
Course Title: Computer Architecture I
Number of credits: 3
Contact Period: 3 hours of lecture per week

2. Course Description:

English: Study of fundamental concepts of logic circuit analysis and design with the aim of understanding and designing the main components of a modern processor. Topics include: Boolean algebra, logic gates, combinational and sequential circuits, arithmetic logic units (ALU), memory and programmable logic devices, data paths, and control units. Practice with logic circuit design problems.

Spanish: Estudio de conceptos fundamentales para el análisis y diseño de circuitos lógicos con el objetivo de entender y diseñar los componentes principales de un procesador moderno. Los temas incluyen: álgebra Booleana, compuertas lógicas, circuitos combinatorios y secuenciales, unidades lógicas aritméticas (ALU), memoria y dispositivos lógicos programables, vías de datos y unidades de control. Práctica con problemas de diseño de componentes lógicos.

3. Pre/Co-requisites and other requirements:

Prerequisites: CIIC 3015 or CIIC 3011 or INGE 3016
Corequisite: INEL 4115

4. Course Objectives:

Students will learn the basic techniques to understand and design logic circuits. Using this knowledge, students will design basic computer components such as logic gates, ALUs, memory banks, and a CPU.

5. Instructional Strategies:

☒conference ☐discussion ☒computation ☐laboratory

☐seminar with formal presentation ☐seminar without formal presentation ☐workshop

☐art workshop ☐practice ☐trip ☐thesis ☐special problems ☐tutoring

☐research ☐other, please specify:

6. Minimum or Required Resources Available:

Students will use the Departmental computer laboratories to complete course projects.

7. Course time frame and thematic outline

Outline	Contact Hours
Combinational logic circuits analysis	6
Combinational logic design	5
Sequential circuit analysis	5
Sequential circuit design	5
Memory and programmable logic devices	7
Register transfers and datapaths	7
Control unit design	7
Exams	3
Total hours: (equivalent to contact period)	45

8. Grading System

☒Quantifiable (letters) ☐ Not Quantifiable

9. Evaluation Strategies

	Quantity	Percent
☒ **Exams**	**3**	**45%**
☒ **Final Exam**	**1**	**30%**
☐ **Short Quizzes**		
☐**Oral Reports**		
☐ **Monographies**		
☐ **Portfolio**		
☒ **Projects**	**1-3**	**25%**
☐**Journals**		
☐**Other, specify:**		
TOTAL:		**100%**

10. Bibliography:

1. M. Morris Mano and Michael Ciletti, *Digital Design*, 5th ed., Prentice Hall, 2012.
2. Charles H. Roth and Larry L Kinney, *Fundamentals of Logic Design*, 7th. ed., Cengage Learning, 2013.
3. David Harris and Sarah Harris, *Digital Design and Computer Architecture*, 2nd ed., Morgan Kaufmann, 2012.

11. Course Outcomes

Upon completion of this course the student will be able to:	Program Outcomes
1. explain the functionality and construct basic combinational logic circuits	C2, E2
2. explain the functionality and construct basic sequential logic circuits	C2, E2
3. analyze the datapath structure of contemporary computer architecture	C1, E1
4. analyze the control unit structure of contemporary computer architecture	C1, E1

12. According to Law 51

Students will identify themselves with the Institution and the instructor of the course for purposes of assessment (exams) accommodations. For more information please call the Student with Disabilities Office which is part of the Dean of Students office (Office #4) at (787)265-3862 or (787)832-4040 extensions 3250 or 3258.

13. Academic Integrity

-The University of Puerto Rico promotes the highest standards of academic and scientific integrity. Article 6.2 of the UPR Students General Bylaws (Board of Trustees Certification 13, 2009-2010) states that academic dishonesty includes, but is not limited to: fraudulent actions; obtaining grades or academic degrees by false or fraudulent simulations; copying the whole or part of the academic work of another person; plagiarizing totally or partially the work of another person; copying all or part of another person answers to the questions of an oral or written exam by taking or getting someone else to take the exam on his/her behalf; as well as enabling and facilitating another person to perform the aforementioned behavior. Any of these behaviors will be subject to disciplinary action in accordance with the disciplinary procedure laid down in the UPR Students General Bylaws.—